# KLI-8811

# 8800 Element Linear CCD Image Sensor

# Performance Specification

**Eastman Kodak Company**
**Image Sensor Solutions**
**Rochester, New York 14650-2010**

**Revision 0**
**October 3, 2000**

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

## TABLE OF CONTENTS



## FIGURES




Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

## 1.1 Features

- User Selectable High Resolution:
  8800 or 7300 active pixels
- High Sensitivity
- Wide Dynamic Range
- No Image Lag
- High Charge Transfer Efficiency
- Up to 1.4V peak-peak Output
- Two-Phase Register Clocking
- On-chip Dark Reference
- 30MHz per channel with Copper/Tungsten package configuration. (120Mhz data rate)

## 1.2 Description

The KLI-8811 is a linear imaging Charge-Coupled Device (CCD) designed for high resolution scanning applications. Each device contains a row of 8800 active photoelements, consisting of high performance pinned diodes for improved sensitivity, lower noise and the elimination of lag. Readout of the pixel data is accomplished through the use of four CCD shift registers, positioned on each side of the photodiode array and divided into left and right halves that read towards the center of the device. The photodiodes are 7µm x 7µm and are located on 7µm centers. The array is structured so as to provide 8 'blank' CCD cells followed by 2200 pixels of active image data for each output. 10 dark reference pixels follow the active pixels, then 4 test pixels, followed by 2 'blank' CCD cells for each output. The user has the option of reducing the resolution to 7300 active pixels by draining the remainder of the charge packets from the shift registers using the resolution select control gate. The devices are manufactured using NMOS, buried channel processing and utilize dual layer polysilicon and dual layer metal technologies. The die size is 63.5 mm X 1.2 mm and is housed in dual-in-line packages in either 0.600" wide, 40-pin cerdip package (see Figure 3), or, 0.400″ wide, cofired ceramic package with a copper-tungsten heat sink (see Figure 4) configurations. The cover glass is Corning 7059 with multi-layer anti-reflective (MAR) coatings.

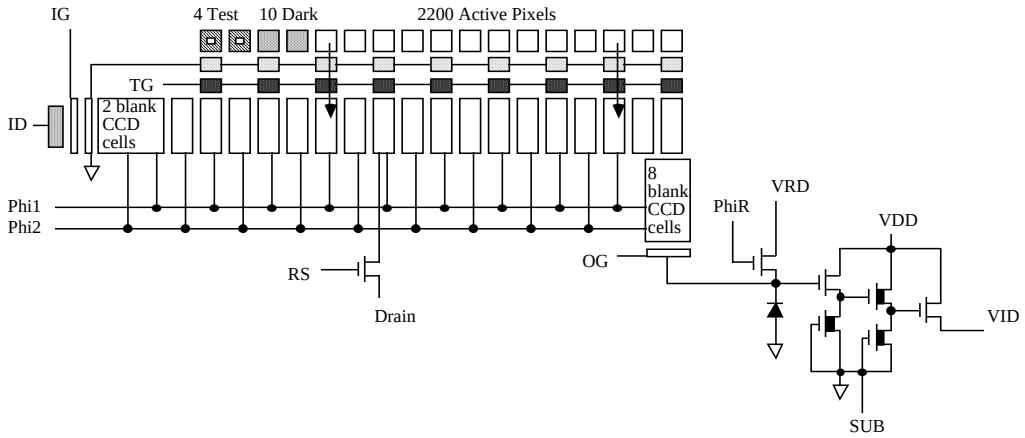



Figure 1 - Single Channel Schematic

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

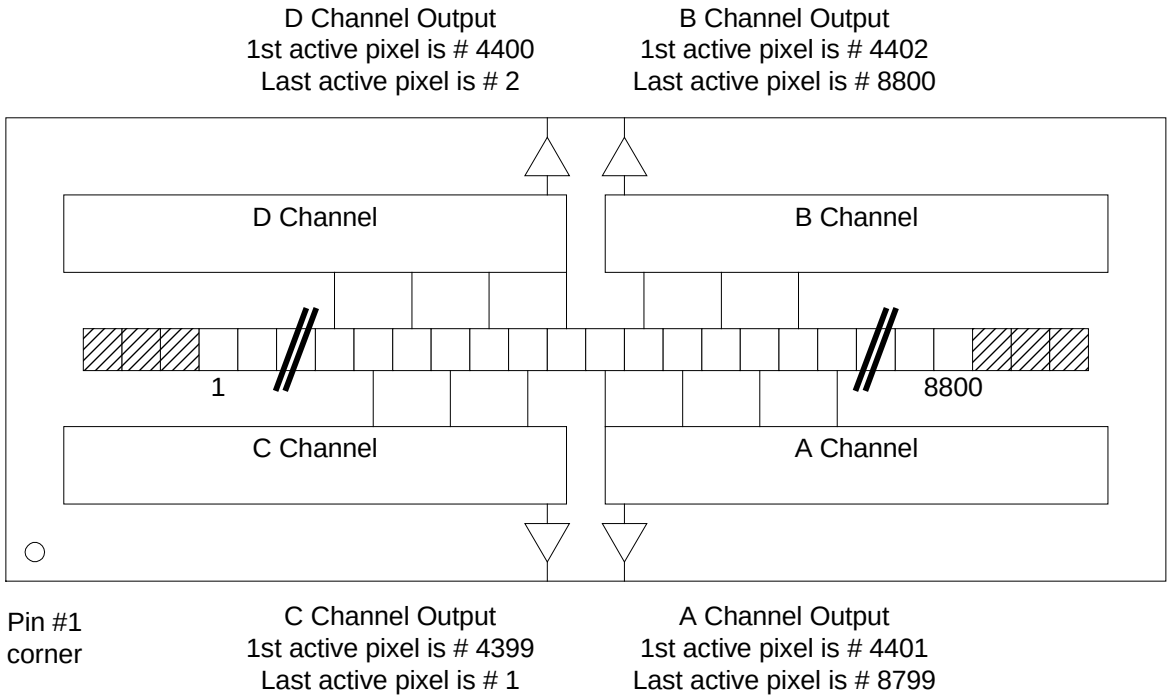



Figure 2 - Functional Block Diagram

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

## 1.3 Imaging

During the integration period, an image is obtained by gathering electrons generated by photons incident upon the photodiodes. The charge collected in the photodiode array is a linear function of the local exposure. Storage of the charge carriers occurs adjacent to the photodiode in the accumulation phase that is self-biased on-chip. Isolation from the CCD shift registers during the integration period is provided by the transfer gate TG, which is held 'off' at a barrier potential. At the end of the integration period, the CCD register clocking is stopped and the H1 shift register clock is turned 'on'. Next, the transfer gate TG is turned 'on' causing the charge to drain from the accumulation phase, through the TG region and into the H1 storage region. Once the transfer is complete, TG is turned 'off' once again to isolate the two regions. Complementary clocking of the H1 and H2 phases subsequently resumes for the readout of the current line of data while the next line of data is integrated.

## 1.4 User-Selectable Resolution

The CCD shift registers are outfitted with a resolution select feature. This feature consists of two control gates labeled RS and H2x. The control gates allow the user to select the high-resolution mode (8800 pixels), or low resolution mode (7300 pixels).

When the RS pin is held at a low potential, (0V), and H2x is connected to H2, the imager will be in the high-resolution mode utilizing all 8800 active pixels.

When the RS pin is held at a high potential, (15V), and H2x is biased to a low potential, (0V), all the charge packets that are clocked into the CCD phase adjacent to the control gate will be emptied of charge carriers. The low resolution mode has the advantage of allowing the clocks to be stopped after the 7300 pixels have been read-out and the next integration period started, thus reducing the line integration time.

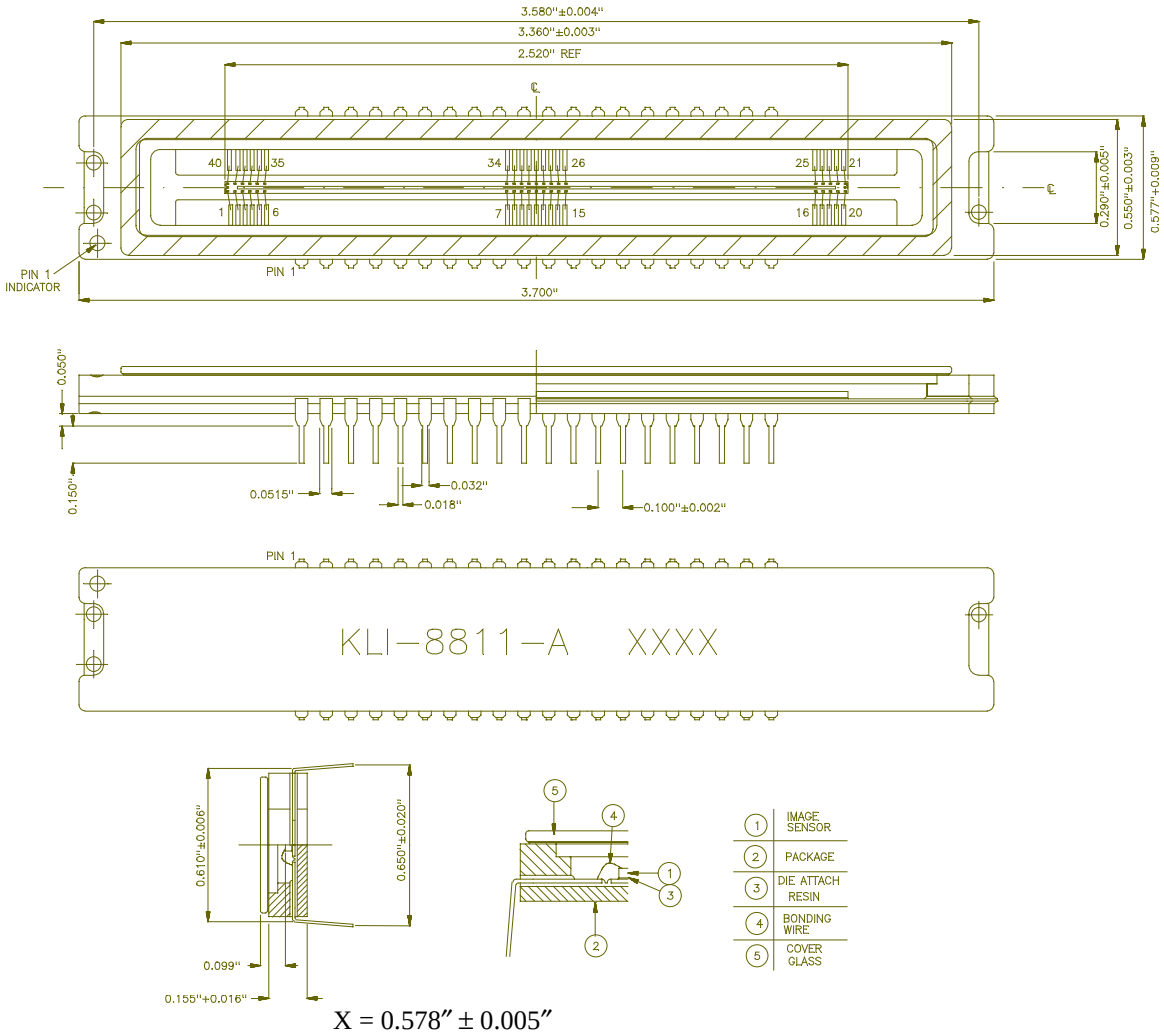
## 1.5 Charge Transport and Sensing

Readout of the signal charge is accomplished by two-phase, complementary clocking of the H1 and H2 gates. The data in all registers is clocked simultaneously toward the output structures. The signal is then transferred to the output structures in a parallel format at the falling edge of the H2 clock. The first active pixel data is available on the ninth H2 falling-edge after the transfer period. Re-settable floating diffusions are used for the charge to voltage conversion while source-followers provide buffering to external connections. The potential change on the floating diffusion is dependent on the amount of signal charge and is given by $\Delta V_{FD} = \Delta Q/C_{FD}$. Prior to each pixel output, the floating diffusion is returned to the $V_{RD}$ level by the reset clock, PHLR. In order to reduce on-chip power dissipation and provide optimum linearity, an off-chip current sink for the third stage source-follower is required for proper operation of the device. (See Operating Conditions.)

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

## 2.1 Package Configurations

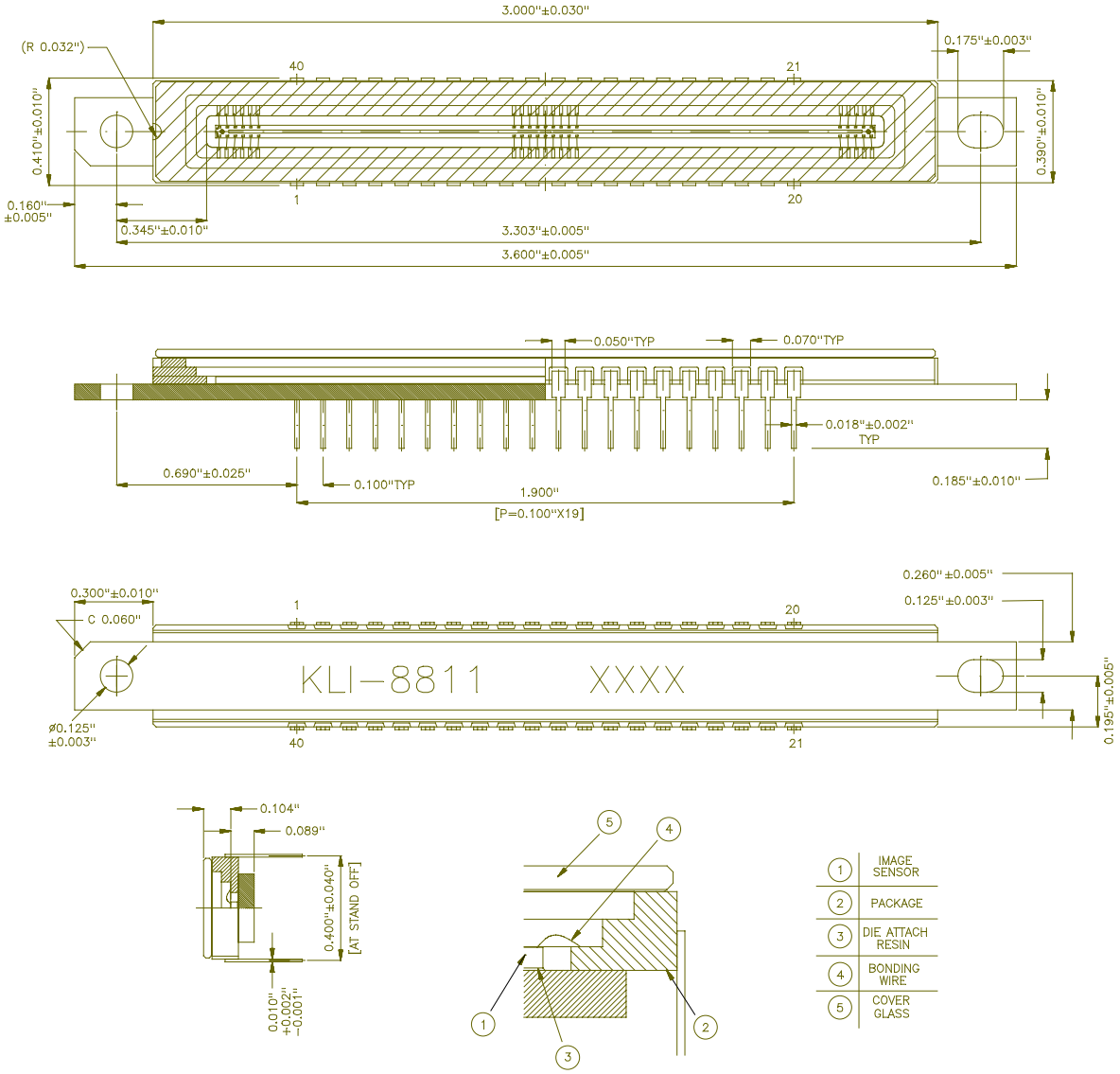
Center of hole in leadframe closest to pin 1 indicator to center of pixel 1:




X = 0.578″ ± 0.005″
Y = 0.100″ ± 0.005″

Figure 3 - Packaging Configuration - Cerdip Package

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com




Center of hole in heatsink at pin 1 end to center of pixel 1:
X = 0.429″ ± 0.005″
Y = 0.000″ ± 0.005″

Figure 4 - Packaging Configuration - Cofired Ceramic Package with Copper/Tungsten Heat Sink

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

## 2.2 Pin Description

| Pin | Symbol | Description |
|---|---|---|
| 1 | H1c | Phase 1 shift register clock (Registers C and D) |
| 2 | H2c | Phase 2 shift register clock (Registers C and D) |
| 3 | TGc | Accumulation phase-to-CCD transfer gate |
| 4 | IG | Electrical Injection input gate test pin |
| 5 | SUB | Substrate connection (ground) |
| 6 | LS | Light shield/scavenger diode |
| 7 | SUB | Substrate connection (ground) |
| 8 | VDD | Output amplifier upper supply |
| 9 | VIDc | Channel 'c' Video Output |
| 10 | PHIR | Sense node reset gate |
| 11 | OG | Shift register output gate bias |
| 12 | VRD | Reset drain bias |
| 13 | VIDa | Channel 'a' Video Output |
| 14 | VDD | Output amplifier upper supply |
| 15 | RS | Resolution Select Control Gate |
| 16 | SUB | Substrate connection (ground) |
| 17 | ID | Electrical Injection input diode test pin |
| 18 | TGa | Accumulation phase-to-CCD transfer gate |
| 19 | H2a | Phase 2 shift register clock (Registers A and B) |
| 20 | H1a | Phase 1 shift register clock (Registers A and B) |
| 21 | N/C | No connection |
| 22 | H2x | Phase 2 or Sub (GND) |
| 23 | TGb | Accumulation phase-to-CCD transfer gate |
| 24 | IG | Electrical Injection input gate test pin |
| 25 | SUB | Substrate connection (ground) |
| 26 | RS | Resolution Select Control Gate |
| 27 | VDD | Output amplifier upper supply |
| 28 | VIDb | Channel 'b' Video Output |
| 29 | VRD | Reset drain bias |
| 30 | OG | Shift register output gate bias |
| 31 | PHIR | Sense node reset gate |
| 32 | VIDd | Channel 'd' Video Output |
| 33 | VDD | Output amplifier upper supply |
| 34 | SUB | Substrate connection (ground) |
| 35 | N/C | No Connection |
| 36 | SUB | Substrate connection (ground) |
| 37 | ID | Electrical Injection input diode test pin |
| 38 | TGd | Accumulation phase-to-CCD transfer gate |
| 39 | H2x | Phase 2 shift register clock, or Sub (GND) |
| 40 | N/C | No connection |

## 2.3 Maximum Ratings

| Parameter | Symbol | Min. | Max. | Units | Remarks |
|---|---|---|---|---|---|
| Gate Pin Voltages | $V_{GATE}$ | 0 | +16 | V | Notes 1, 2 |
| Pin to Pin Voltage | $V_{PIN-PIN}$ | 0 | 16 | V | Notes 1, 3 |
| Diode Pin Voltages | $V_{DIODE}$ | -0.5 | +16 | V | Notes 1, 4 |
| Output Bias Current | $I_{DD}$ | --- | -10 | mA | Note 5 |
| Output Load Capacitance | $C_{VID,LOAD}$ | --- | 15 | pF | |
| CCD Clocking Frequency | $f_{CLK}$ | --- | 30 | MHz | Notes 6, 8 |
| Operating Temperature | $T_{OP}$ | 0 | +70 | $^oC$ | Note 7 |
| Storage Temperature | $T_{ST}$ | -25 | +80 | $^oC$ | |

**Notes:**
1. Referenced to substrate voltage.
2. Includes pins: H1n, H2n, TGn, PHIR, OG, IG, and RS.
3. Voltage difference (either polarity) between any two pins.
4. Includes pins: VIDn, VRD, VDD, LS and ID.
5. Care must be taken not to short output pins to ground during operation as this may cause serious damage to the output structures.
6. Charge transfer efficiency will degrade at frequencies higher than the nominal clocking frequency.
7. Noise performance will degrade with increasing temperatures.
8. 30 MHz operation requires the CuW package; $f_{clk}$max = 15MHz for the cerdip package. Data rate is 4x the CCD clock rate

**CAUTION: To allow for maximum performance, this device contains limited Electrostatic Discharge (ESD) protection. Although all gate pins are protected, Standard Class I ESD prevention handling procedures should be followed at all times!**

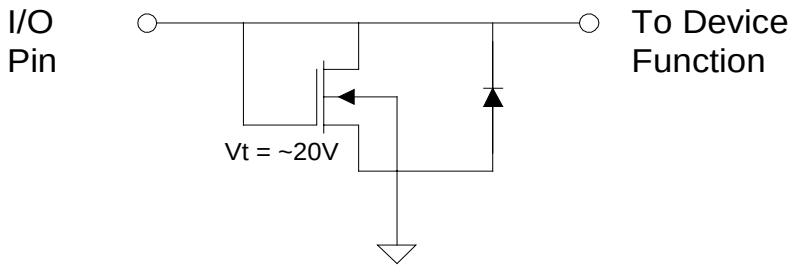


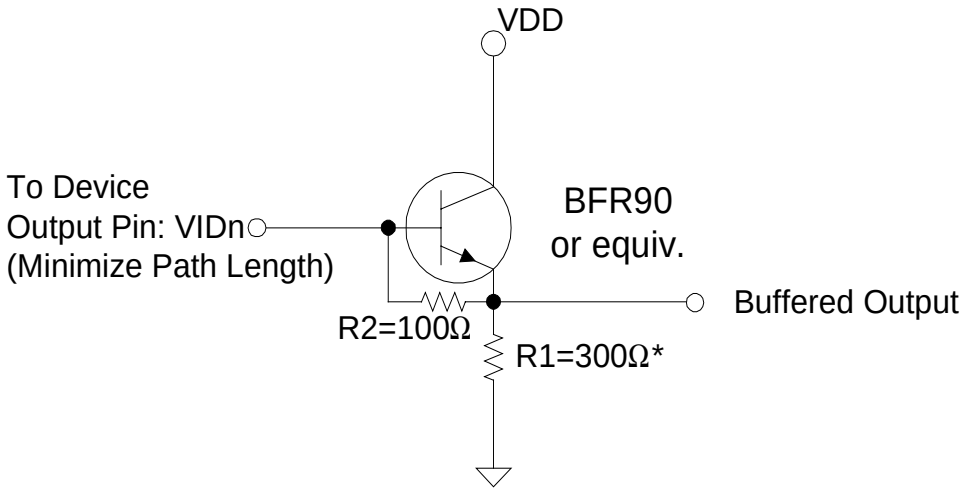

Figure 5 - ESD Protection Circuit

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

## 2.4 DC Conditions

| Symbol | Parameter | Min. | Nom. | Max. | Units | Remarks |
|---|---|---|---|---|---|---|
| SUB | Substrate | -- | 0 | -- | V | (Ground) |
| RS | High Resolution Select | -0.5 | 0 | 0 | V | Note 1 |
| RS | Low Resolution Select | +13 | +15 | +15.5 | V | Note 2 |
| VRD | Reset Drain Bias | +11 | +11.2 | +11.8 | V | Note 3 |
| VDD | Output Buffer Supply | +13 | +15 | +15.5 | V | |
| Iddn | Output Bias Current / Chan. | -- | -7.0 | -- | mA | Note 4 |
| OG | Output Gate Bias | 0 | 0 | +0.5 | V | |
| LS | Light Shield/Drain Bias | +13 | +15 | +15.5 | V | |
| IG | Test Pin-Input Gate | --- | 0 | --- | V | |
| ID | Test Pin-Input Diode | +13 | +15 | +15.5 | V | |

**Notes:**
1. Bias RS to this level for 8800 pixel resolution. (See AC conditions for H2X biasing.)
2. Bias RS to this level for 7300 pixel resolution. (See AC conditions for H2X biasing.)
3. This parameter has a direct impact on the saturation voltage and the DC offset of the device.
4. An off-chip current sink must be supplied for each output. Load capacitance should be minimized so as not to limit bandwidth. See example below.




Choose values optimized for specific operating frequency.

Figure 6 Typical Output Bias/Buffer Circuit

## 2.5 AC Clock Level Conditions

| Symbol | Parameter | Min. | Nom. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| VH1H, VH2H, VH2xH | CCD Readout Clocks High | +6.25 | +6.5 | +7.0 | V | 2 |
| VH1L, VH2L, VH2xL | CCD Readout Clocks Low | -0.1 | 0 | +0.1 | V | 1, 2 |
| VTGH | Transfer Clock High | +6.25 | +6.5 | +7.0 | V | |
| VTGL | Transfer Clock Low | -0.1 | 0 | +0.1 | V | 1 |
| VPHIRH | Reset Clock High | +6.25 | +6.5 | +7.0 | V | |
| VPHIRL | Reset Clock Low | -0.1 | 0 | +0.1 | V | 1 |
| VH2X | Low Resolution Mode | - | 0 | - | V | 2 |

**Notes:**
1. Care should be taken to insure that low rail overshoot does not exceed -0.5 VDC. Exceeding this value may result in non-photo-generated charge being injected into the video signal.
2. For the High Resolution mode H2x is connected to the phase 2 clock; for the Low Resolution mode H2x is connected to substrate (ground).

## 2.6 Clock Line Capacitance

| Symbol | Parameter | Min. | Nom. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| $C_{H1n}$ | Phase 1 Clock Capacitance | | 260 | | pF | 1 |
| $C_{H2n}$ | Phase 2 Clock Capacitance | | 300 | | pF | 1 |
| $C_{TGn}$ | Transfer Gate Capacitance | | 60 | | pF | |
| $C_{PHIR}$ | Reset Gate Capacitance | | 30 | | pF | |

**Notes:**
1. This is the total load capacitance per phase pin.

Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

## 2.7 AC Timing

| | | Pixel Clock Rate | | | | |
|---|---|---|---|---|---|---|
| Symbol | Parameter | 30 MHz | 15 MHz. | 2 MHz | Units | Remarks |
| $1e = 1/f_{CLK}$ | CCD Element Duration | 33.3 | 66.7 | 500 | ns | |
| $1L = t_{intHR}$ | Line/Integration Period High Resolution Mode | 75.2 | 150.4 | 1128 | µs | Note 1 |
| $1L = t_{intLR}$ | Line/Integration Period Low Resolution Mode | 62.17 | 124.3 | 932.5 | µs | Note 2 |
| $t_r$ | Clock Rise Time | --- | --- | 8 | ns | |
| $t_{prop}$ | Clock to Video Edge Delay | --- | --- | 4 | ns | |
| $\tau_{ac}$ | Accum.-to-H1 Transfer | 1 | --- | --- | µs | |
| $\tau_{tg}$ | TG Gate Clear | 66.7 | --- | --- | ns | |
| $t_{rst}$ | Reset Pulse Duration | 6 | --- | --- | ns | |
| $t_{cd}$ | Clamp to H2 Delay | 5 | --- | --- | ns | Note 3 |
| $t_{sd}$ | Sample to Reset Edge Delay | 5 | --- | --- | ns | Note 3 |

**Notes:**
1. Assumes minimum of 2256 clock cycles per line: $(8+2200+10+4+2+30(t_{ac})+2(t_{tg})) = 2256$.
2. Assumes minimum of 1865 clock cycles per line: $(8+1825+30(t_{ac})+2(t_{tg})) = 1865$.
3. Recommended delays for correlated double sampling (CDS) signal processing.

(15 MHz Operation taken at the CCD video output with 1.5V Signal)

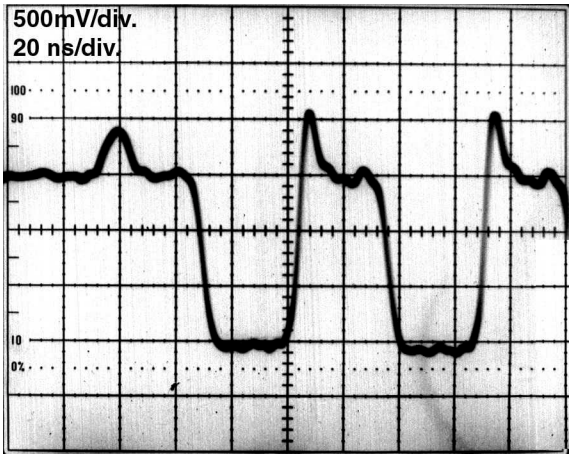
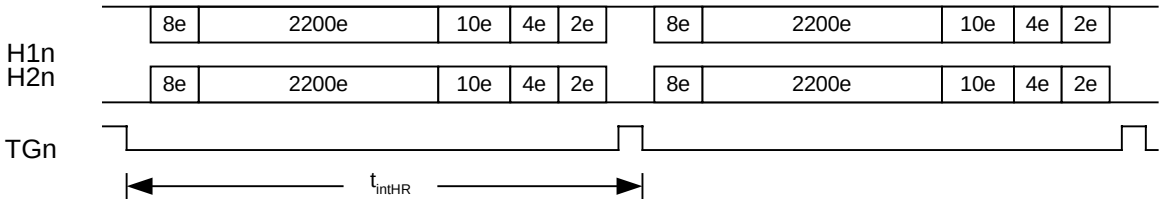



Figure 7 - Output Waveforms

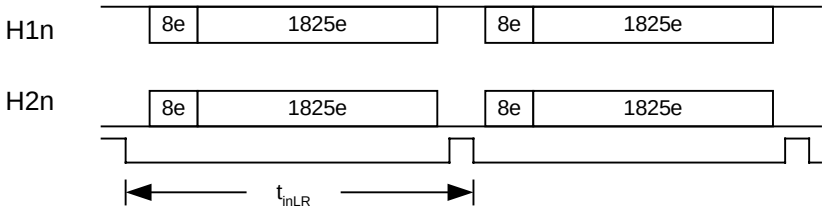
Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

### 2.7.1 Timing Diagram

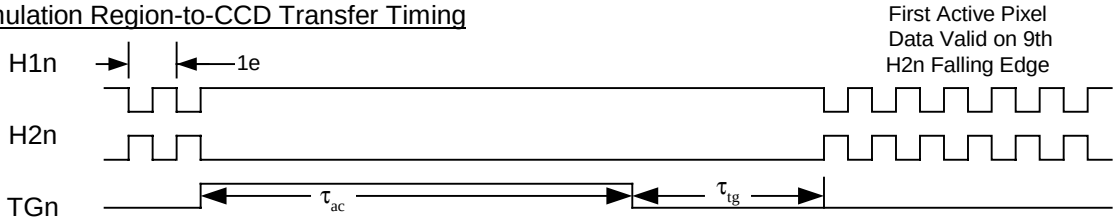
Line Timing - High resolution Mode (RS set to 0 Volts, H2x tied to H2)



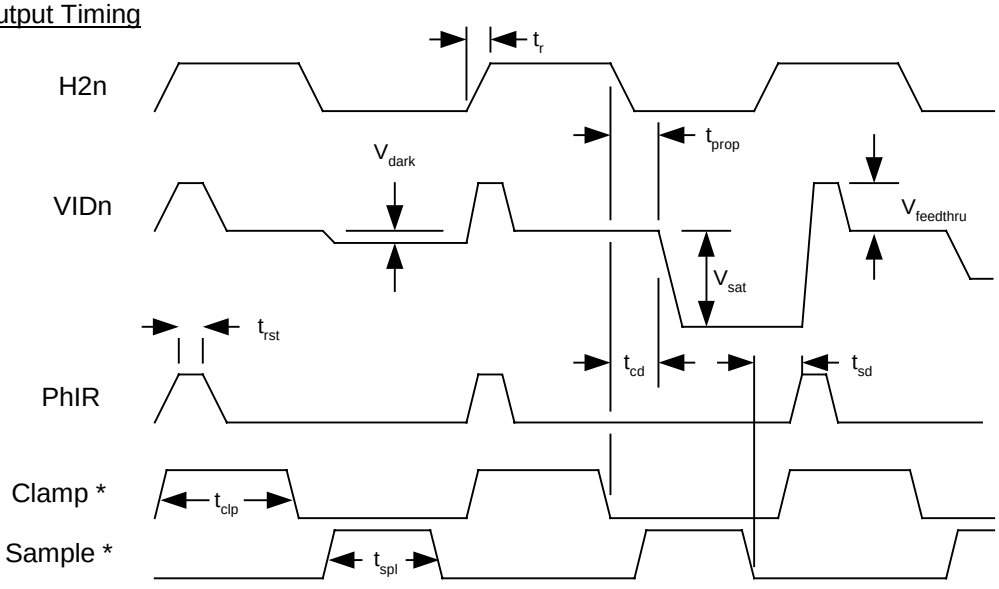

Line Timing - Low resolution Mode (RS set to +15 Volts, H2x set to 0 Volts)




Accumulation Region-to-CCD Transfer Timing




Output Timing




* Optional Off-Chip Analog Correlated Double Sampling (CDS) Signal Processing Clocks

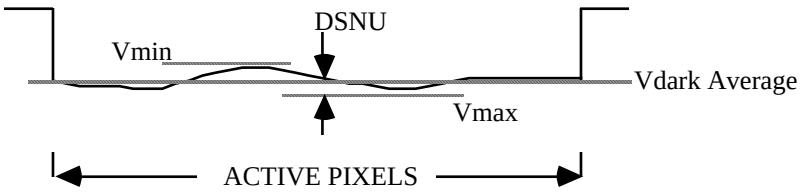
Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

## 3.1 Image Specifications

Operating conditions: 25°C ambient, $f_{CLK}$ = 2 MHz and nominal external load.

| Symbol | Parameter | Min. | Nom. | Max. | Units | Remarks |
|---|---|---|---|---|---|---|
| $V_{SAT}$ | Saturation Output Voltage | 1.0 | 1.4 | --- | $V_{p-p}$ | Notes 1, 7 |
| $\Delta V_o/\Delta N_e$ | Output Sensitivity | --- | 12.0 | --- | µV/e- | |
| $N_{e,sat}$ | Saturation Signal Charge | --- | 100k | --- | e- | |
| *R* | Responsivity | | 14.0 | | $V/\mu J/cm^2$ | Note 2 |
| $R_{out}$ | Amplifier Output Resistance | --- | 110 | --- | Ω | Note 3 |
| DR | Dynamic Range | --- | 70 | --- | dB | Notes 4, 10 |
| $I_{dark}$ | Dark Current | --- | 0.01 | --- | pA | Notes 5, 10 |
| DSNU | Dark Signal Non-Uniformity | | 1.5 | 3.0 | mV | Note 10 |
| CTE, η | Charge Transfer Efficiency | .99990 | 99999 | --- | - | Notes 6, 10 |
| *L* | Lag | --- | --- | 1 | % | 1st Field, Note 10 |
| $V_{o,DC}$ | Video Output DC Offset | 6.5 | 8.5 | 10.5 | V | Note 7 |
| PRNU | Response Non-uniformity | --- | --- | ±10 | % | Note 8 |
| Ne,dark | RMS Dark Noise | --- | <50 | --- | e- | Note 9 |
| PD | On-Chip Power Dissipation | --- | 1.5<br>300 | --- | W, AC<br>mW, DC | |
| $V_{RES}$ | Residual Signal in Low Resolution mode Drained Pixels | --- | --- | 1.0 | mV | Note 10 |

**Notes:**
1. Defined as the maximum output level achievable before linearity or PRNU performance is degraded.
2. Measured at 550 nm with MAR coated 7059 cover glass. Typical response curve shown in later section.
3. Increasing external VIDn load current (nominally -7mA) to improve signal bandwidth will decrease these parameters.
4. This device utilizes 2-phase clocking for cancellation of driver displacement currents. Symmetry between H1n and H2n phases must be maintained to minimize clock noise.
5. Dark current doubles approximately every +9°C.
6. Measured per transfer. For total line h $<(.99999)^{2256} = 0.978$.
7. This parameter is dependent on the value of Vrd.
8. Low frequency response (>20 pixels) across array.
9. Measured at integration time (tint) = 10.0 msec, temperature extrapolated to 22°C.
10. Operating at frequency higher than specified will result in a degradation in this parameter.




Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

### 3.1.1 Device Responsivity

Note:
1. It is recommended that a suitable IR cut filter be used to optimize MTF while minimizing smear.

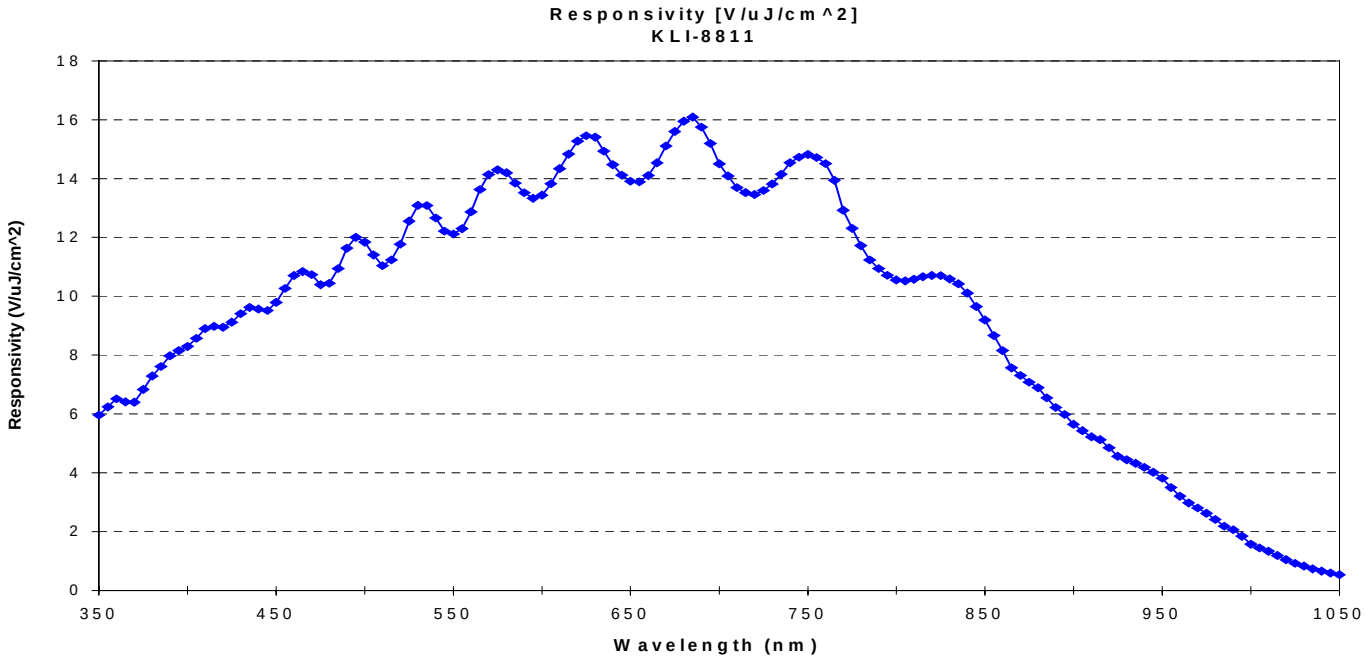
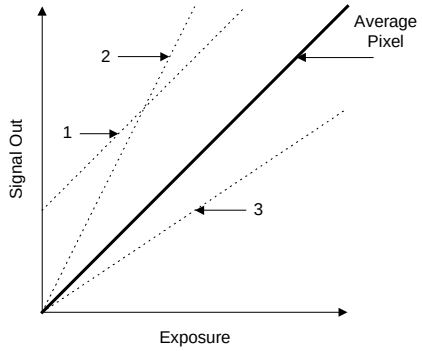



Figure 8 Typical Responsivity

## 3.2 Defect Classification (Test conditions: T=25ºC, $f_{CLK}$=2MHz)

| Field | Defect Type | Threshold | Units | Number | Remarks |
|---|---|---|---|---|---|
| Dark | Bright | 10 | mV | 0 | Notes 1, 2 |
| Bright | Bright/Dark | 20 | % | 6 | Notes 1, 3, 4 |

**Notes:**
1. Defective pixels will be separated by at least one non-defective pixel within and across channels.
2. Pixels whose response is greater than the average response by the specified threshold. See line 1 in the figure.
3. Pixels whose response is greater or less than the average response by the specified threshold. See lines 2 and 3 in the figure.
4. Defective pixels to be separated by at least 1000 good pixels.




Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

## 4.1 Quality Assurance and Reliability

4.1.1 Quality Strategy: All devices will conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and inspection at key points of the production process. Typical limits are not a guarantee but provided as a design target.

4.1.2 Replacement: All devices are warranted against failures in accordance with the Terms of Sale.

4.1.3 Devices are shipped free of any mobile contamination and scratches that are within the imager pixel area and the corresponding glass region directly above the pixel sites. Inspection is performed under magnification to verify the internal cavity of the imager complies. The topside of the device glass is highly susceptible to particles and contamination. Touching the CCD window must be avoided when handling. Wear soft gloves free of grease, oil, or lint. Use a soft lens brush to remove dust. A soft cloth (must be lint free) to remove stubborn dirt. For exceptional cases of grease stains on the cover glass, a soft cloth and 99% alcohol or methanol can be used.

4.1.4 ESD Precautions: Devices are shipped in static-safe containers and should only be handled at static-safe workstations.

4.1.5 Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request.

4.1.6 Test Data Retention: Devices have an identifying number traceable to a test data file. Test data is kept for a period of 2 years after date of shipment.

## 4.2 Ordering Information

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (716) 722-4385
Fax: (716) 477-4947

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

**WARNING: LIFE SUPPORT APPLICATIONS POLICY**

Image Sensor Solutions, Eastman Kodak Company products are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury to persons or property or other consequential damages.